

WG7A01E01A

WG7A01-01 2.4G Wi-Fi/BLE Sip Module

SDIO (uSD/TF) Adapter Board

User Guide

D 0.1

| Prepared By | Reviewed By | Approved By |
|-------------|-------------|-------------|
| | | |

Index

| | |
|---------------------------------------------|-----------|
| 1. INTRODUCTION..... | 2 |
| 2. HARDWARE DESCRIPTION | 3 |
| 2.1 WG7A01E01A BOARD OVERVIEW | 3 |
| 2.2 CONNECTOR AND JUMPER DESCRIPTIONS | 4 |
| 2.3 POWER..... | 6 |
| 2.4 CLOCKING | 6 |
| 2.5 PERFORMING CONDUCTED TESTING | 6 |
| 3. SCHEMATIC DIAGRAMS | 8 |
| 4. DIMENSION | 10 |
| 5. HISTORY CHANGE..... | 10 |

1. INTRODUCTION

The WG7A01-01 is a 2.4GHz Wi-Fi 6 and Bluetooth® Low Energy module, enable affordable, reliable and secure connectivity in embedded applications with a processor host running Linux® or an MCU host running RTOS.

The following WG7A01E01A kit is available:

The WG7A01E01A is SDIO (uSD/TF) adapter board with 2.4GHz Wi-Fi/BT module solutions for NXP i.MX RT and i.MX 6 / 7 / 8 / 9 Evaluation Kits.

- WG7A01-01 LGA-100 package development platform
- Wi-Fi through uSD interface
- BLE through UART interface

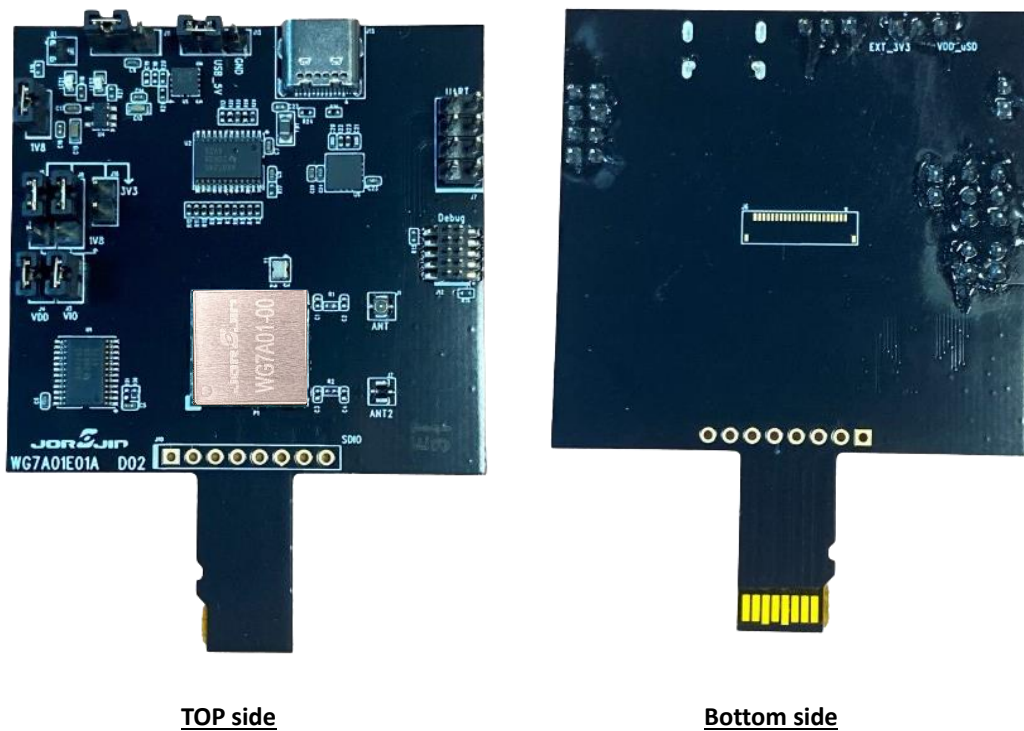


Figure 1-1. WB2072-00 BLE wireless MCU Module Evaluation Kit

2. HARDWARE DESCRIPTION

2.1 WG7A01E01A board overview

Hardware features:

- WG7A01-01 Wi-Fi 6 and Bluetooth® Low Energy combo module which can interface with MPU or MCU systems adding connectivity
- Onn-board U.FL connector for conducted RF testing
- Power from on board dual LDO (3.3 V and 1.8 V) using USB or uSD
- 2 level shifters for voltage translation (3.3 V to 1.8 V)
- JTAG header pins for SWD interface with XDS110
- Jumper for current measurement on both power supplies (3.3 V and 1.8 V)
- 32 kHz oscillator for lower power evaluation

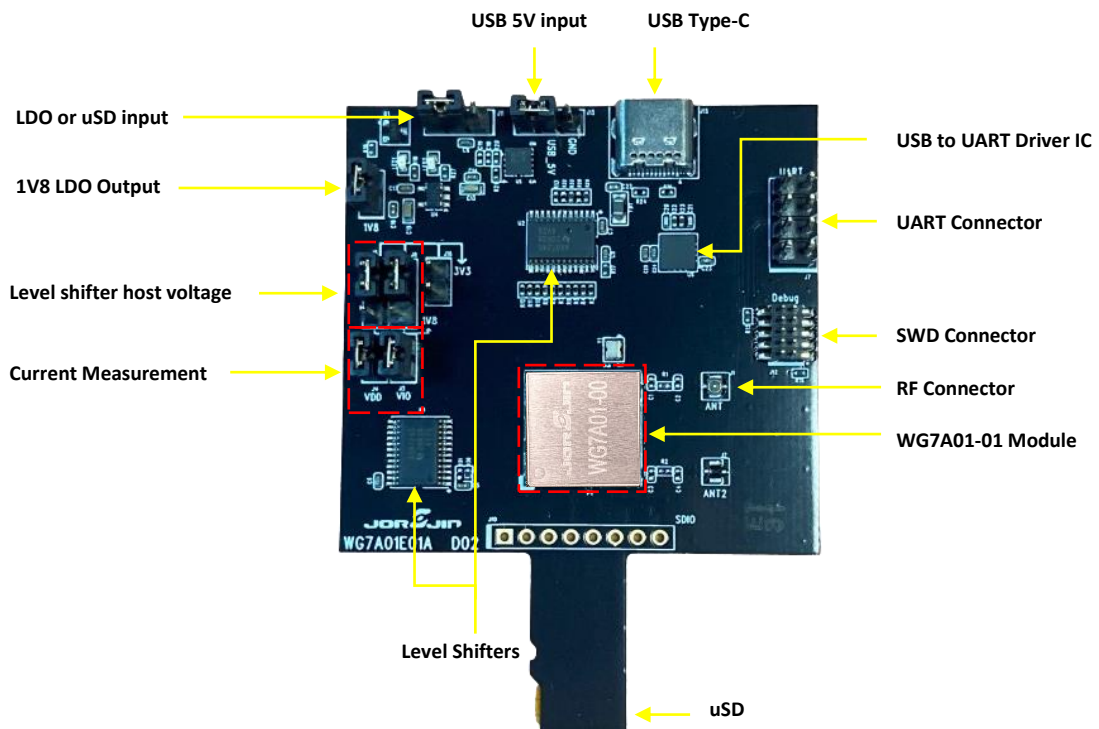


Figure 2-1. Hardware description of Evaluation Kit

2.2 Connector and Jumper Descriptions

2.2.1 LED Indicators:

Table 2-1. LEDs

| Reference | Color | Usage | Comments |
|-----------|-------|-----------------------|------------------------------------------------------------|
| LED1 | Green | 1.8V power indication | On: 1.8V power rail is up. Off: no 1.8V power supplied. |
| LED2 | Red | 3.3V power indication | On: 3.3V power rail is up. Off: no 3.3V power supplied. |

2.2.2 Jumper Settings

Table 2-2 lists the jumper settings. To reference the default jumper configurations, see [Figure 2-1](#).

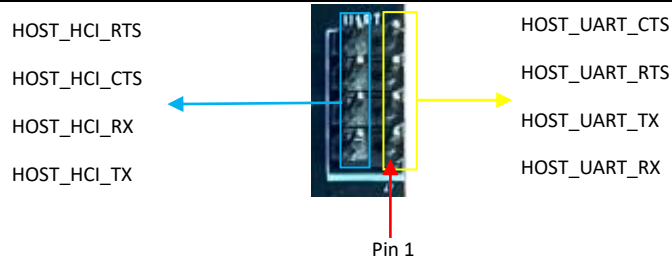
Table 2-2. Jumper Settings

| Reference | Usage | Comments |
|-----------|----------------------------|-----------------------------------------------------------------------------------------------------|
| J1,J2 | RF Test | U.FL connector (J1) for conducted testing in the lab. |
| J3,J4 | Current measurement | Used to measure power to module only. |
| J5,J8 | Level shifter host voltage | Set to 3.3 V or 1.8 V to enable relevant level shifters to translate to correct host voltage level. |
| J6 | FPC connectors | FPC connector for UART and other control signal. |
| J7 | UART connectors | Embedded UART-to-USB IC as an option for UART. |
| J9,J10 | Micro-SD (uSD) | Micro-SD (uSD) interface for Wi-Fi. |
| J11 | Power to board | Set LDO for 3V3 supply, connector J11 (1-2) Set uSD for 3V3 supply, connector J11 (2-3) |
| J12 | SWD connectors | Headers to interface with XDS110 debug probe |
| J13 | Power to board | Set USB 5V input |
| J14 | Power to board | Set LDO 1V8 output |
| J15 | USB connector | USB supply and UART-to-USB IC enable |
| J16 | Power to board | Set FPC 3V3 input |

2.2.3 UART Headers

Table 2-3. Jumper Settings

| pin | Signal Name | pin | Signal Name |
|------|---------------|------|--------------|
| J7.1 | HOST_UART_RX | J7.2 | HOST_HCI_TX |
| J7.3 | HOST_UART_TX | J7.4 | HOST_HCI_RX |
| J7.5 | HOST_UART_RTS | J7.6 | HOST_HCI_CTS |
| J7.7 | HOST_UART_CTS | J7.8 | HOST_HCI_RTS |



2.2.4 FPC Connector

Table 2-4. Jumper Settings

| pin | Signal Name | pin | Signal Name |
|-------|--------------------|-------|-------------------|
| J6.1 | HOST_COEX_REQ | J6.11 | HOST_LOGGER |
| J6.2 | HOST_COEX_GRANT | J6.12 | HOST_FAST_CLK_REQ |
| J6.3 | GND | J6.13 | HOST_ANT_SEL |
| J6.4 | GND | J6.14 | VDD_3V3_FPC |
| J6.5 | HOST_COEX_PRIORITY | J6.15 | VDD_3V3_FPC |
| J6.6 | HOST_SLOW_CLK_IN | J6.16 | HOST_UART_RX |
| J6.7 | HOST_IRQ_WL | J6.17 | HOST_UART_CTS |
| J6.8 | GND | J6.18 | HOST_UART_TX |
| J6.9 | HOST_IRQ_BLE | J6.19 | HOST_UART_RTS |
| J6.10 | HOST_RESET | J6.20 | GND |

2.2.5 SWD Headers

The WG7A01E01 was designed with SWD headers (J12) for SWD interface with the XDS110 debug probe. The signal assignment for these headers are described in the figures and tables below.

The main SWD interface for the WG7A01E01 is via the XDS110 that is connected to the 10pin header (J12), however this header is not populated with the default kit.

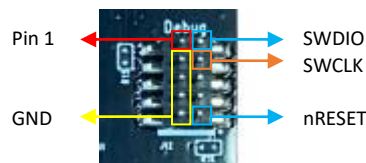


Figure 2-2. ARM 10 pin JTAG Connector (J12)

Table 2-3. ARM 10 pin SWD Connector (J12) Assignment

| pin | Signal Name | Description |
|--------|-------------|------------------------------------------------|
| J12.1 | VCC_BRD_1V8 | 1.8V supply for reference voltage to connector |
| J12.2 | SWDIO | Serial wire data in/out |
| J2.4 | SWCLK | Serial wire clock |
| J12.10 | RESET_1V8 | nReset (Enable line for WG7A01-01) |

| | | |
|----------------------------|-----|--------------|
| J12.3, J12.5, J12.7, J12.9 | GND | Board ground |
|----------------------------|-----|--------------|

2.3 Power

The board is designed to accept power from a connected uSD socket, the USB connector (J15) on the WG7A01E01A can be used to aid in extra current. The jumpers labeled J14 (1.8-V) and J11 (3.3-V) can be used to measure the total current consumption of the board from the onboard LDO.

2.3.1 Low Current Measurement (LPDS)

To measure the current draw of the WG7A01-01 module for both power supplies (3.3 V or 1.8 V), a jumper labeled J4 (for 3.3 V supply) and a jumper labeled J3 (for 1.8 V supply) is provided on the board. By removing J4, users can place an ammeter into this path to observe the current on the 3.3 V supply. The same process can be used for observing the current on the 1.8 V supply with J3

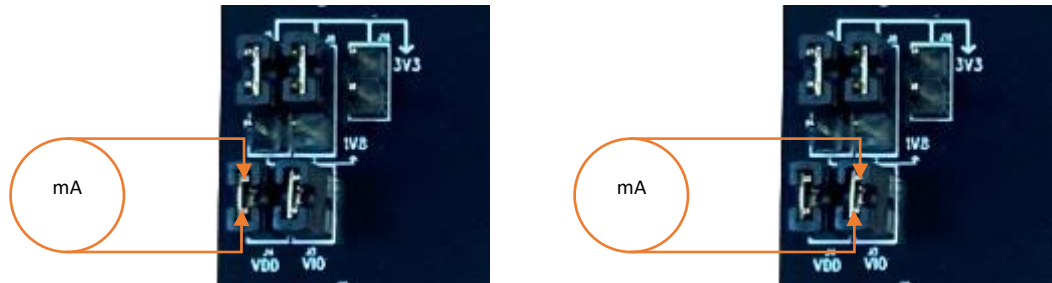


Figure 2-3. Low Current Measurement

2.4 Clocking

- Y1 is a 32.768 kHz oscillator for slow clock input.

If the user desires to provide their own external slow clock through the Slow Clock Input pin (J6.6), then some re-work must be performed. The Y1 oscillator needs to be removed, and populate a 0201 sized, 0 ohm resistor on R13 pad. See Figure 2-4. The slow clock can also be generated internally to save on BOM.

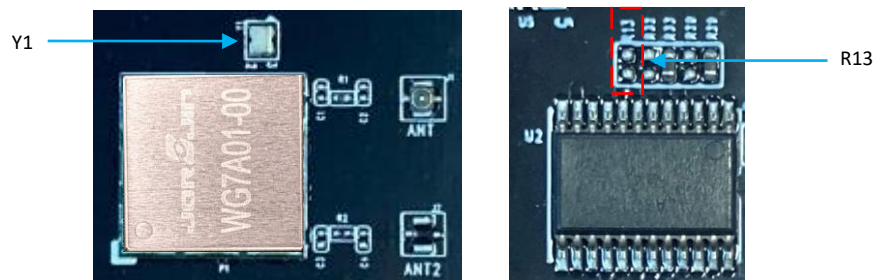


Figure 2-4. 32.768KHz Clock

2.5 Performing Conducted Testing

As seen in Figure 2-5, the WG7A01E01A has an on-board U.FL connector. The U.FL connector (J1) provides a way for testing conducted measurements.

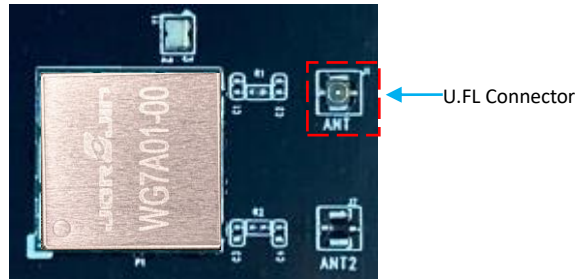


Figure 2-5. U.FL Connector

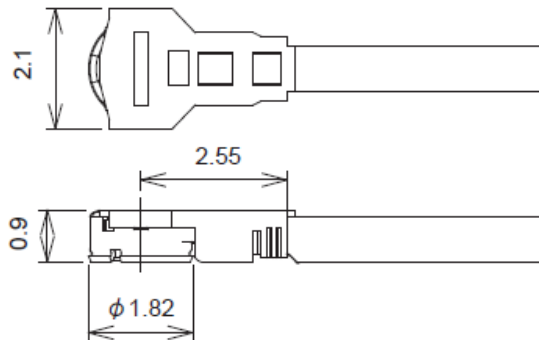
MHF® 4 Plug Cable Assembly

Mating profile : **1.2mm MAX.**

Applicable for AWG36 ($\phi 0.81\text{mm}$) Cable

Plug P/N: 20448-001R-081

【Applicable Cable gauge】



| | |
|-----------------------------------|-----------------------|
| Part No. (Au) | 20448-001R-081 |
| Part No. (Ag) | - |
| for AWG#36 | |
| | |
| Braided Shield of Outer Conductor | Single Braided Shield |

3. SCHEMATIC DIAGRAMS

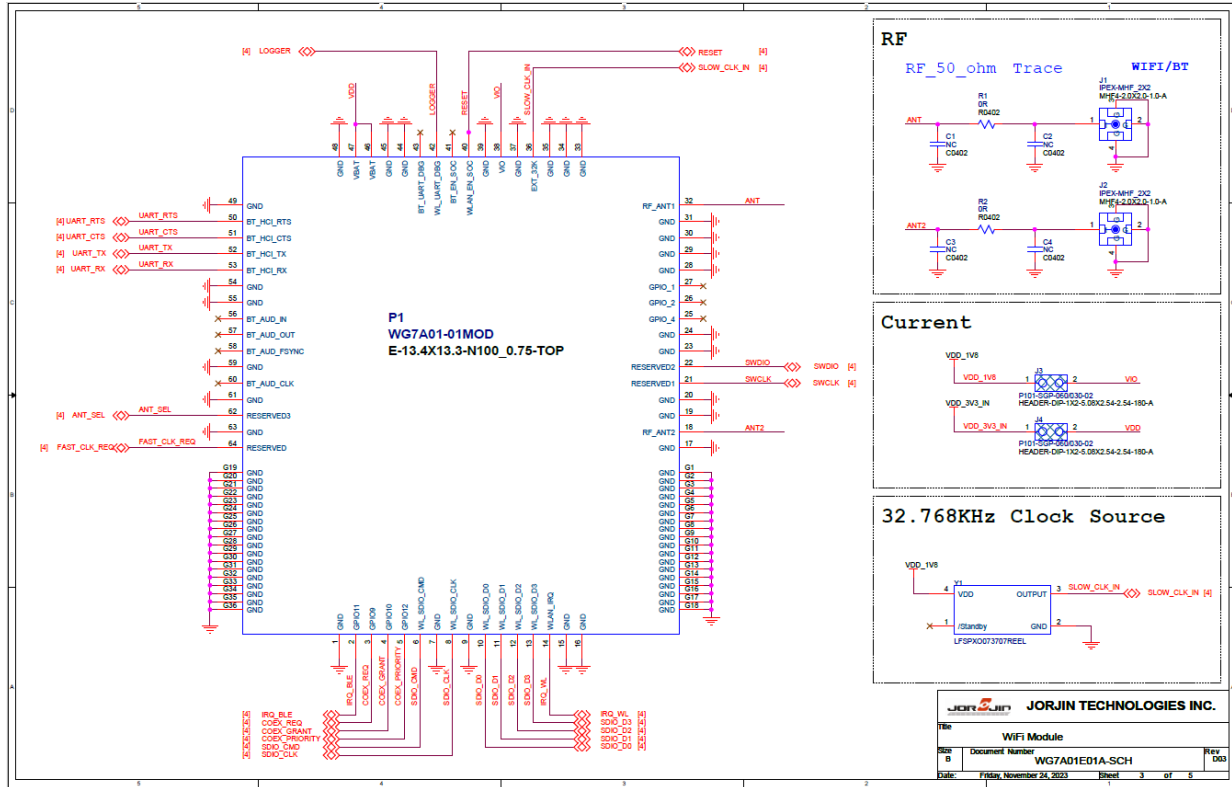


Figure 3-1. WG7A01E01A circuit schematic (1 of 3)

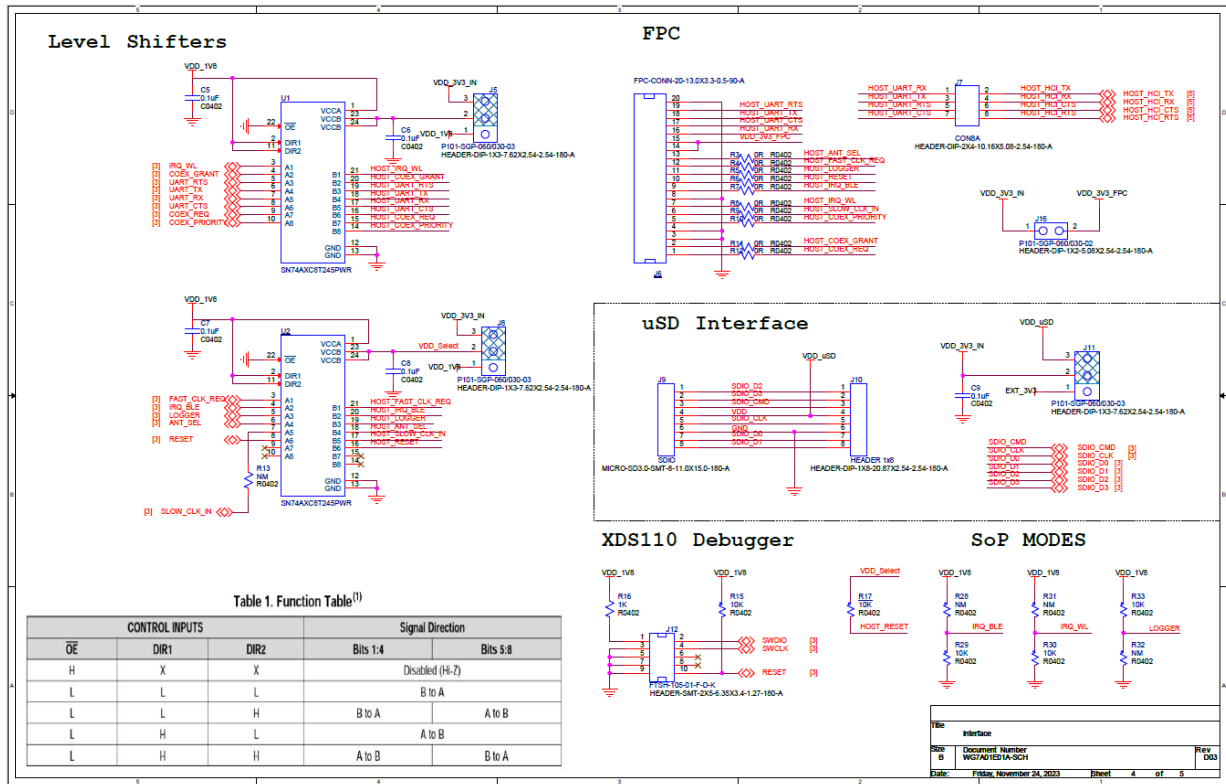


Figure 3-1. WG7A01E01A circuit schematic (2 of 3)

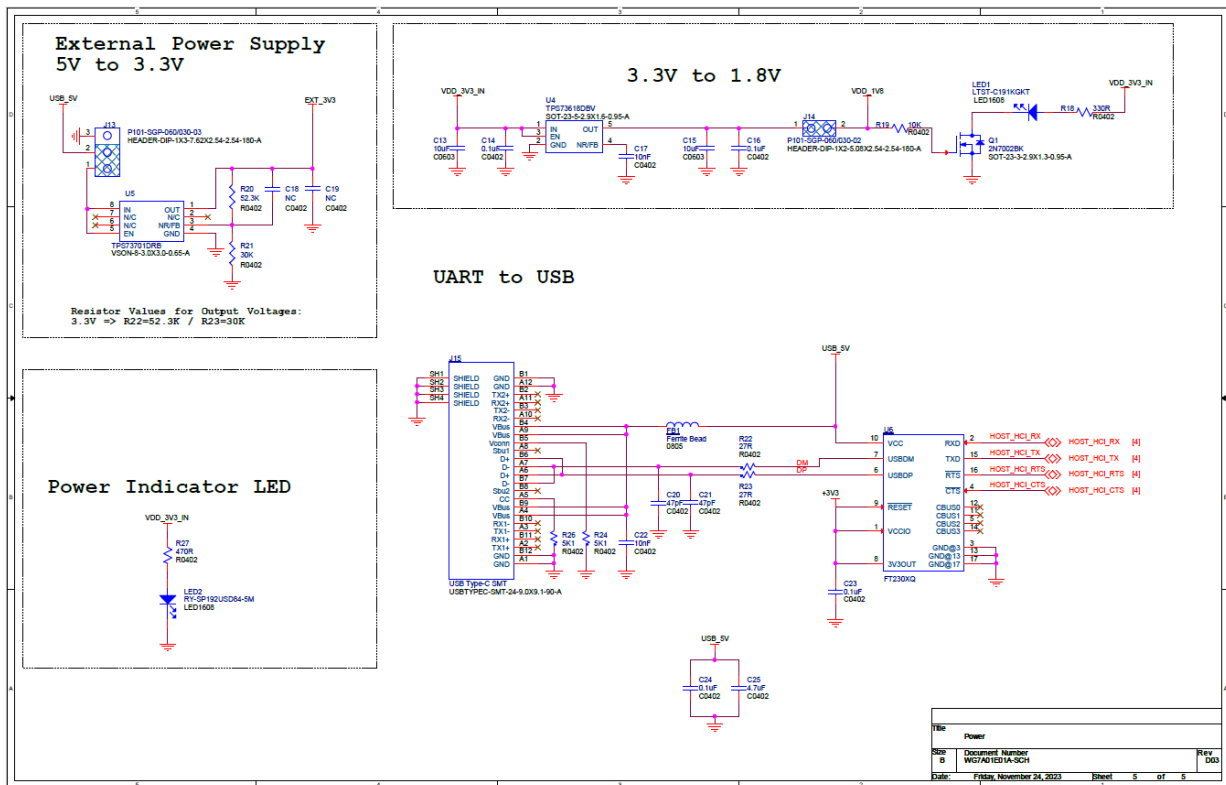


Figure 3-1. WG7A01E01A circuit schematic (3 of 3)

4. DIMENSION

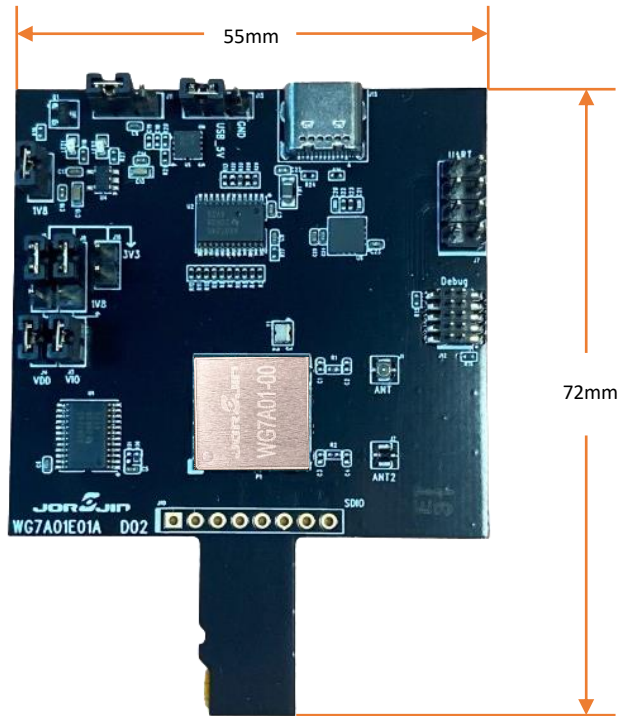


Figure 4-1. Board Dimension

5. HISTORY CHANGE

| Revision | Date | Description |
|-----------|------------|---------------------------------------------------------------------------------------|
| Draft 0.1 | 2023-12-27 | Draft version. |
| D01 | 2024-05-10 | 1. Add 2.2.3 UART headers illustrate 2. Add MHF® 4 Plug Cable Assembly information |
| | | |